#5 / Pre Amedt A
6-18-03

XA-9593

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Takashi KOBAYASHI et al

Intl. Appln. No.: PCT/JP00/06146

Intl. Filing Date: 8 September 2000

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND PROCESS FOR PRODUCING THE SAME

* * *

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above-identified patent application as indicated below.

IN THE CLAIMS:

9. (Amended) A process according to any one of Claims 1-5, 7, or 8, wherein the third gates are self-aligned to the floating gates.

A1